AMENDMENTS TO THE SPECIFICATION

Please replace paragraph **[0018]** with the following amended paragraph:

[0018] In the drawings, like or similar elements are designated with identical reference numerals throughout the several views thereof, and the various elements depicted are not necessarily drawn to scale. Referring now to FIG. 1, depicted therein is a conventional PI-model representation for deriving an RC netlist for a memory circuit 100. A plurality of memory cells organized as an array and various global signal lines associated therewith (e.g., bitlines and wordlines) are modeled as resistive and capacitive loadings that span horizontally or vertically. Reference numerals 80-1, 80-2 and 80-3 exemplify three global lines in the array's X-direction. Similarly, reference numerals [[82-1, 82-1 and 82-3]] ~~exemplify three~~ 82-1 and 82-2 exemplify two global lines in Y-direction of the array.

Please replace paragraph **[0026]** with the following amended paragraph:

[0026] Corresponding to the rows of the bitcell tiles, X-DEC 104 is also segmented into a plurality of vertically-stacked row decoder tiles. In the exemplary embodiment depicted in FIG. [[1]] 2A, row decoder tile 112-1 corresponds to the row 109A of bitcell tiles 110-3 and 110-4. In similar fashion, row decoder tile 112-2 corresponds to the row 109B of bitcell tiles 110-1 and 110-2.

Please replace paragraph **[0032]** with the following amended paragraph:

[0032] Furthermore, similar to the WL arrangement described hereinabove, the segmented BLs are operable to be coupled in a head-to-tail fashion from one tile to another along the vertical direction by virtue of a second plurality of appropriately defined I/O pins associated with the tiles. In the exemplary embodiment depicted in FIG. 2B, the 32 BLs 231-1 provided with respect to the I/O block tile 208-1 are operable to be coupled to the corresponding 32 input pins 232-0 through 232-31 of the bitcell

array tile 202-11 via a suitable MUX8 arrangement. In turn, the bitcell array tile 202-11 is provided with 32 output pins in the vertical direction (reference numerals 234-0 through 234-31) with respect to the 32 global BLs, which output pins are operable to be coupled to the corresponding input pins 236-0 through 236-31 of the next bitcell array tile (i.e., tile 202-21) in the tile column. Similarly, output pins 238-0 through 238-31 are defined for the bitcell array tile [[202-1]] 202-21 regarding the BLs 231-1 for connecting to the input pins 240-0 through 240-31 of the bitcell array tile 202-31 that is stacked above the bitcell array tile 202-21. Reference numerals 242-0 through 242-31 refer to the output pins of the bitcell array tile 202-31 for connecting with the next bitcell array tile in the array tile matrix with reference to the global BL signals 231-1.

Please replace paragraph **[0034]** with the following amended paragraph:

[0034] Within the complex of the tiles as set forth above, each tile is modeled with appropriate RC elements that accurately represents the parametric loading associated with that particular tile. In accordance with the teachings of the present invention,

the tile-specific RC elements are then connected together because of the I/O pins provided for the tiles. In other words, for each tile, an RC element is disposed between its input and output pins that correspond to a particular global line. For instance, with reference to bitcell array tile 202-11, an RC element (RCWL) is disposed between input pin 252-15 and the corresponding output pint 254-15, an RC element between input pin [[252-15]] 252-14 and the corresponding output pin 254-14, and so on for the remaining 14 I/O pin pairs. As mentioned above, the output pins of the bitcell array tile 202-11 are connected to the input pins of the bitcell array tile 202-12, referring to the global signals in X-direction. In similar manner, appropriate RC elements (RCBL) are provided for the bitcell array tiles with respect to the global signals in Y-direction. Furthermore, appropriate RC elements are provided for the X-DEC and I/O block tiles, which are operable to be stitched together in Y-direction and X-direction, respectively.